What is claimed is:

1. An apparatus for converting a differential signal to a single-ended output signal, wherein the apparatus is operated from first and second power supplies, the apparatus comprising:

a differential pair circuit that is configured to provide an intermediate signal in response to the differential signal;

a current mirror circuit that is coupled to the differential pair circuit such that the current mirror circuit is a load for the differential pair circuit, wherein the current mirror circuit is arranged such that a voltage associated with the intermediate signal approximately corresponds to an arithmetic mean of the first power supply voltage and the second power supply voltage; and

a first current source circuit that is coupled to the differential pair circuit such that the first current source provides a tail current to the differential pair circuit; and

a trans-impedance circuit that is configured to operate from the first power supply voltage and the second power supply voltage, wherein the trans-impedance stage comprises:

a first inverter circuit having a first inverter input and a first inverter output, wherein the first inverter input is configured to receive the intermediate signal and the first inverter output is configured to provide an output signal that is responsive to the intermediate signal;

a first transistor having a first gate, a first drain, and a first source, wherein the first gate is coupled to the first inverter output, the first drain is coupled to the first power supply, and the first source is coupled to the first inverter input, and

a second transistor having a second gate, a second drain, and a second source, wherein the second gate is coupled to the first inverter output, the second drain is coupled to the second power supply, and the second source is coupled to the first inverter input.

2. The apparatus of Claim 1 further comprising: a second current source and a third current source, wherein the current mirror circuit comprises a third transistor and a fourth transistor, wherein the fourth transistor is arranged to operate as a diode, wherein the second current source is configured to provide a first current to the third transistor, such that a drain-to-source voltage associated with the third transistor is maintained, and wherein the third current source is configured to provide a second current to the fourth transistor such that current mirror is operable for higher speed differential signals.

3. The apparatus of Claim 2, further comprising a bias circuit that is arranged to adjust the tail current, the first current, and the second current in response to a common-mode voltage associated with the differential signal.

4. The apparatus of Claim 2, further comprising a bias circuit that is arranged to provide a bias signal in response to a common-mode voltage associated with the differential signal, wherein the differential pair circuit comprises a fifth transistor and a sixth transistor that include common sources that are coupled to the first current source, wherein the first current source includes a seventh transistor, the second current source includes an eighth transistor, and the third current source includes a ninth transistor, wherein the seventh, eighth, and ninth transistors are biased by the bias signal, wherein the bias circuit comprises a tenth transistor, an eleventh transistor, and a twelfth transistor, wherein the gate of the tenth transistor is coupled to the bias signal, and the drain of the tenth transistor is coupled to the sources of the eleventh and twelfth transistors, and wherein the gates associated with the fifth, sixth, eleventh, and twelfth transistors are associated with the differential signal.

5. An apparatus for converting a differential signal to a single-ended output signal, wherein the apparatus is operated from first and second power supplies, the apparatus comprising:

an operational trans-conductance amplifier having an amplifier input and an amplifier output, wherein: the operational trans-conductance amplifier is configured to operate from the first power supply and the second power supply, the amplifier input is

arranged to receive the differential signal, and the amplifier output is arranged to provide an intermediate signal that is responsive to the differential signal; and

a trans-impedance stage that is configured to operate from the first and second power supplies, wherein the trans-impedance stage is arranged in cooperation with the operational trans-conductance amplifier such that a voltage associated with the intermediate signal approximately corresponds to an arithmetic mean of the first and second power supplies, wherein the trans-impedance stage comprises:

a first inverter circuit having a first inverter input that is coupled to the amplifier output, and a first inverter output that is configured to provide an output signal that is responsive to the intermediate signal;

a first transistor having a first gate that is coupled to the output signal, a first drain that is coupled to the first power supply, and a first source that is coupled to the first inverter input; and

a second transistor having a second gate that is coupled to the output signal, a second drain that is coupled to the second power supply, and a second source that is coupled to the first inverter input.

6. The apparatus of Claim 5, wherein the first inverter circuit comprises at least one of an inverter gate and a NAND gate.

7. The apparatus of Claim 5 further comprising a buffer circuit, wherein the buffer circuit is configured to buffer the output signal to provide a buffered output signal.

8. The apparatus of Claim 7, wherein the buffer circuit comprises at least one of an inverter and a Schmitt trigger.

9. The apparatus of Claim 5,

wherein the operational trans-conductance amplifier circuit comprises:

a differential pair circuit comprising a third transistor and a fourth transistor, wherein the differential pair is configured to receive the differential signal;

a current mirror circuit comprising a fifth transistor and a sixth transistor, wherein the sixth transistor is configured to operate as a diode; and

a first current source that is configured to provide a tail current to the differential pair; and

the apparatus further comprising a second current source that is configured to provide a current to the sixth transistor at least when the fourth transistor is inactive such that the operational trans-conductance amplifier is operable for rapid polarity changes in the differential signal.

10. The apparatus of Claim 5:

wherein the operational trans-conductance amplifier circuit comprises:

a differential pair circuit comprising a third transistor and a fourth transistor, wherein the differential pair is configured to receive the differential signal, wherein the third and fourth transistors have third and fourth gates and drains, respectively;

a current mirror circuit comprising a fifth transistor and a sixth transistor, wherein the sixth transistor is configured to operate as a diode; and

a first current source that is configured to provide a tail current to the differential pair, wherein the first current source comprises a seventh transistor having a seventh gate and a seventh source; and

the apparatus further comprising:

an eighth transistor having an eighth gate that is coupled to the seventh gate, an eighth source is coupled to the seventh source, and an eighth drain;

a ninth transistor having a ninth gate that is coupled to the fourth drain, a ninth source that is coupled to the eighth drain, and a ninth drain that is coupled to the eighth gate; and

a tenth transistor having a tenth gate that is coupled to the third gate, a tenth source that is coupled to the ninth source, and a tenth drain that is coupled to the eighth gate.

11. The apparatus of Claim 5, wherein the first transistor is an n-type transistor and the second transistor is a p-type transistor.

12. The apparatus of Claim 5, wherein the inverter circuit is sized to reduce current associated with the output signal.

13. The apparatus of Claim 5, wherein a voltage difference associated with the first power supply and the second power supply corresponds to approximately 2.5 volts.

14. An apparatus for converting a differential signal to a single-ended output signal, wherein the apparatus is operated from first and second power supplies, the apparatus comprising:

an operational trans-conductance means that is configured to provide a current to an intermediate node in response to the differential signal; and

a trans-impedance means that is configured to provide an output voltage in response to the current such that the output voltage corresponds to: a sum of a voltage level and a gate-to-source voltage of a first transistor when the current has a negative polarity, a difference of the voltage level and a gate-to-source voltage of a second transistor when the current has a positive polarity, wherein the operational trans-conductance amplifier and the trans-impedance means are arranged in cooperation with one another such that a voltage associated with the intermediate node approximately corresponds to a mid-supply voltage.

15. The apparatus of Claim 14, wherein a voltage difference between the first power supply and the second power supply corresponds to approximately 2.5 volts, and wherein the voltage level corresponds to approximately the half of the voltage difference.

16. The apparatus of Claim 14, further comprising a means for buffering that is configured to buffer the output signal to provide a buffered output signal.

17. The apparatus of Claim 14, wherein the trans-impedance means comprises:

a means for inverting that is configured to provide the output signal in response to an intermediate signal associated with the intermediate node by applying an inverting gain;

a first means for following that is configured to maintain the gate-to-source voltage between the intermediate signal and the output voltage when the first means for following is active, wherein the first means for following is active when the current has a negative polarity; and

a second means for following that is configured to maintain the gate-to-source voltage between the intermediate signal and the output voltage when the second means for following is active, wherein the second means for following is active when the current has a positive polarity.

18. The apparatus of Claim 15, further comprising a current source means that is arranged to maintain the operational trans-conductance means during high-speed operation.

19. The apparatus of Claim 18, further comprising a biasing means that is arranged to adjust currents in the trans-conductance means and the current source means in response to a common-mode voltage that is associated with the differential signal..

20. The apparatus of claim 15, further comprising another operational trans-conductance means that is configured to provide another current to the intermediate node in response to the differential signal, wherein the operational trans-conductance means is arranged to operate a common-mode range, the other operational trans-conductance means is arranged to operate over another common-mode range, and the operational trans-conductance means and the other operational trans-conductance means are arranged to cooperate with one another to provide an intermediate signal at the intermediate node.